PATENT
Attorney Docket No. H1102C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Shibly S. Ahmed et al.	)	Group Art Unit: 2822
	)	
Serial No.: 10/720,166	)	Examiner: M. Wilczewski
	)	
Filed: November 25, 2003	)	
	)	
For: DOUBLE GATE SEMICONDUCTOR DEVICE HAVING A METAL GATE	)	
	)	

APPEAL BRIEF

U.S. Patent and Trademark Office
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Sir:

This Appeal Brief is submitted in response to the Final Office Action mailed April 6, 2006 and in support of the Notice of Appeal filed July 6, 2006.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 37, 39-42, 46-54, 56 and 57 are pending in this application and are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the Final Office Action mailed April 6, 2006.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Each of the independent claims involved in this appeal is recited below, followed in parenthesis by examples of where support can be found in the specification and drawings for the claimed subject matter. In addition, each dependent claim argued separately below is also summarized.

Claim 37 recites: A semiconductor device, comprising: a substrate (page 5, paragraph 29; Fig. 1, 110); an insulating layer formed on the substrate (page 5, paragraph 29; Fig. 1, 120); a conductive fin formed on the insulating layer, the conductive fin including a plurality of side surfaces and a top surface (page 6, paragraphs 33-34; Figs. 2A-2B, 210); a source region formed on the insulating layer adjacent a first end of the conductive fin (page 6, paragraph 34; Fig. 2A, 220); a drain region formed on the insulating layer adjacent a second end of the conductive fin (page 6, paragraph 34; Fig. 2A; 230); a dielectric layer comprising hafnium formed on the top surface and side surfaces of the conductive fin in the channel region of the semiconductor device (page 10, paragraph 46; Fig. 8, 810); and a metal gate formed on the insulating layer adjacent the

conductive fin in a channel region of the semiconductor device, the metal gate having a thickness ranging from about 700 Å to about 2,000 Å (page 7, paragraph 38; page 10, paragraph 47; Fig. 8, 820).

Claim 41 recites: A semiconductor device, comprising: a substrate (page 5, paragraph 29; Fig. 1, 110); an insulating layer formed on the substrate (page 5, paragraph 29; Fig. 1, 120); a silicon fin formed on the insulating layer, the silicon fin including a plurality of side surfaces and a top surface (page 6, paragraphs 33-34; Figs. 2A-2B, 210); a dielectric layer comprising hafnium formed on the top surface and side surfaces of the silicon fin in the channel region of the semiconductor device (page 10, paragraph 46; Fig. 8, 810); a source region formed on the insulating layer adjacent a first end of the silicon fin (page 6, paragraph 34; Fig. 2A, 220); a drain region formed on the insulating layer adjacent a second end of the silicon fin (page 6, paragraph 34; Fig. 2A, 230); and a metal gate formed on the insulating layer adjacent the silicon fin in a channel region of the semiconductor device, the metal gate having a thickness ranging from about 700 Å to about 2,000 Å (page 7, paragraph 38; page 10, paragraph 47; Fig. 8, 820).

Claim 47 recites: The semiconductor device of claim 41, wherein the dielectric layer comprises HfSiO (page 10, paragraph 46).

Claim 49 recites: The semiconductor device of claim 48, wherein the metal gate comprises a titanium nitride (page 10, paragraph 47).

Claim 51 recites: The semiconductor device of claim 50, wherein the metal gate comprises a tantalum nitride (page 10, paragraph 47).

Claim 52 recites: A semiconductor device, comprising: a substrate (page 5, paragraph 29; Fig. 1, 110); an insulating layer formed on the substrate (page 5, paragraph 29; Fig. 1, 120); a conductive fin formed on the insulating layer, the conductive fin including a plurality of side surfaces and a top surface and having a thickness ranging from about 300 Å to about 1,500 Å (page 5, paragraph 30; page 6, paragraphs 33-34; Figs. 2B, 130); a dielectric layer comprising hafnium formed on the top surface and side surfaces of the silicon fin (page 10, paragraph 46; Fig. 8, 810); a source region formed on the insulating layer adjacent a first end of the silicon fin (page 6, paragraph 34; Fig. 2A, 220); a drain region formed on the insulating layer adjacent a second end of the silicon fin (page 6, paragraph 34; Fig. 2A, 230); and a metal gate comprising titanium or tantalum formed on the insulating layer and over a portion of the conductive fin, the metal gate having a thickness ranging from about 700 Å to about 2000 Å (page 7, paragraph 38; page 10, paragraph 47; Fig. 8, 820).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 37, 39-42, 46-54, 56 and 57 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fried et al. (U.S. Patent No. 6,583,469; hereinafter Fried) in view of Yeo et al. (U.S. Patent No. 6,855,990; hereinafter Yeo).

VII. ARGUMENT

A. Rejection under 35 U.S.C. § 103 based on Fried and Yeo

1. Claims 37, 39-42, 46, 48, 50 and 52-54

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

With these principles in mind, claim 37 recites a semiconductor device that includes a conductive fin formed on an insulating layer, the conductive fin including a plurality of side surfaces and a top surface. Claim 37 also recites a dielectric layer comprising hafnium formed on the top surface and side surfaces of the conductive fin in the channel region of the semiconductor device. As to this feature, the Final Office Action admits that Fried does not disclose or suggest this feature, but states that Yeo discloses a semiconductor device having a fin with an overlying gate in which the gate dielectric layer comprises a high dielectric constant material, such as hafnium oxide and points to Fig. 2 and col. 3, lines 20-39 and col. 7, lines 4-15 for support (Final Office Action – page 3). The Final Office Action further states that it would have been obvious to substitute a material comprising hafnium for the gate dielectric layer of Fried (Final Office Action – pages 3-4). Appellants respectfully disagree.

Fried discloses utilizing a conventional thermal growth process to form the gate dielectric. Fried further discloses that the thermal growth process may include an oxidation, nitridation or oxynitridation (Fried – col. 6, lines 30-35). Such a thermal growth process, as disclosed in Fried, is clearly not compatible with forming a gate dielectric layer that comprises hafnium, as required by claim 37. Therefore, Appellants assert that modifying Fried's gate dielectric layer comprising an oxide, nitride, oxynitride or combination thereof with a dielectric layer comprising hafnium would be a significant change to the processing described in Fried. Appellants further assert that such a modification would not have been obvious based on the disclosure of Yeo.

For example, Yeo may disclose forming a gate dielectric layer that comprises hafnium. However, the Final Office Action has not provided any objective motivation as to why it would

have been obvious to replace a conventional thermal growth process used to form a gate dielectric in Fried with a process that includes forming a gate dielectric layer that comprises hafnium. The Final Office Action merely states that it would have been obvious and does not point to any portion of either reference as providing objective motivation for modifying Fried to include the feature of Yeo (Office Action – page 5). Appellants respectfully assert that it would not have been obvious to modify Fried to include features from Yeo due to the incompatible nature of the process disclosed by Fried and that disclosed by Yeo. In other words, Fried specifically discloses forming a gate dielectric layer using a thermal growth process. Using a thermal growth process to form a dielectric layer is not at all similar to forming a dielectric layer comprising hafnium, as disclosed in Yeo. Therefore, Appellants respectfully assert that it would not have been obvious to combine features from Yeo with Fried absent impermissible hindsight.

In response to similar arguments made in the previous response, the Final Office Action states that Yeo is deemed to be a teaching of the functional equivalence of an oxide, oxynitride or hafnium-containing layer as a gate dielectric in a FinFET device (Final Office Action – page 4). Appellants assert, however, that some objective motivation must exist for features from Yeo to be combined with Fried. In other words, the mere fact that one reference allegedly provides some missing disclosure with respect to a claim does not satisfy the requirements of 35 U.S.C. § 103 as to why it would have been obvious to combine the references. Appellants assert that it would not have been obvious to combine these two references without the benefit of Appellants' disclosure. Moreover, the fact that the modification to Fried (alleged to be obvious) would amount to a significant change in the processing of Fried supports Appellants' assertion that such a modification would not have been obvious without the benefit of Appellants' disclosure.

Claim 37 also recites that the semiconductor device includes a metal gate formed on the insulating layer adjacent the conductive fin in a channel region of the semiconductor device, the metal gate having a thickness ranging from about 700 Å to about 2,000 Å. The Final Office Action states that Fried discloses forming a metal gate 32 on the insulating layer and points to col. 6, lines 39-52 and col. 3, line 55 to col. 4 for support (Final Office Action – page 2). Fried may disclose forming a gate electrode 32 as illustrated in Fig. 18B. Fried, however, is totally silent with respect to the thickness of gate electrode 32. Absent some disclosure with respect to the thickness of gate electrode 32 in Fried, Appellants assert that Fried cannot be fairly construed to disclose or suggest that gate electrode 32 is formed to the thickness recited in claim 37. Yeo also does not disclose or suggest this feature.

In response to similar arguments made in the previous response, the Final Office Action states that Fig. 17B of Fried shows that gate electrode 32 has a thickness about equal to that of fin 12 and oxide layer 16 (Final Office Action – pages 4-5). The Final Office Action further states that Fried discloses that fin 12 has a thickness of 300 to 2000 Å and hard mask 14 has a thickness of about 100 to 1000 Å and therefore, the thickness of gate electrode 32 is about 400 to 3000 Å (Final Office Action – page 5). Appellants respectfully disagree.

Initially, Appellants note that Fig. 17B of Fried is a schematic illustration and is not drawn to scale. In addition, Fig. 17B of Fried illustrates that gate electrode 32 is formed at its lower portion from the recess formed in insulating layer 10u (described at col. 5, line 64 to col. 6, line 8 and illustrated in Fig. 13B) to the top of insulating material 20. The top portion of gate electrode 32 in Fig. 17B is parallel to a portion of oxide layer 16. Appellants assert that it is not possible to discern any particular thickness of gate electrode 32 from Fig. 17B and the

corresponding portions of Fried, much less that the thickness of gate electrode 32 is about 400 to 3000 Å, as alleged in the Final Office Action.

For example, Fried at col. 6, lines 4-8 discloses that the controlled oxide reaction (COR) etching process removes some of the insulating layer 10u beneath the semiconductor body to create a recessed area, as illustrated in Fig. 12B. Fried does not disclose the depth of the recessed area formed in layer 10u, only that a portion of layer 10u is recessed. This recess is also illustrated in Fig. 17B and is filled by the material forming gate electrode 32. Therefore, this recess clearly affects the thickness of gate electrode 32 and is not defined in Fried to be any particular thickness.

In addition, as discussed above, Fig. 17B of Fried is only a schematic representation of the device and is not drawn to any scale. Therefore, it is impossible to determine the thickness of the gate electrode 32 above the top portion of fin 12. That is, the top portion of gate electrode 32 is illustrated as being formed at a level that is parallel to some portion of oxide layer 16. Fried, as mentioned in the Final Office Action, states that hard mask 14, which includes oxide layer 16 and nitride layer 18 has a thickness of about 100 Å to about 1000 Å (Fried – col. 4, lines 1-8). Fried, however, is totally silent with respect to the thickness of oxide layer 16, which forms part of the hard mask 14. Further, as discussed above, Fig. 17B of Fried illustrates that gate electrode 32 is formed at a level that is above the lower portion of oxide layer 16 and below the top of oxide layer 16. Since it is not possible to determine the thickness of oxide layer 16 based on the disclosure of Fried, it is therefore also impossible to determine the thickness of this upper portion of gate electrode 32 which is formed at a level that is planar with some portion of oxide layer 16.

Based on the lack of disclosure in Fried regarding the thickness of gate electrode 32, Appellants assert that the statement in the Final Office regarding the thickness of gate electrode 32 (i.e., that the thickness of gate electrode ranges from 400 to 3000 Å) is based on mere speculation and is not supported by the actual disclosure of Fried. Therefore, Appellants maintain that Fried cannot be fairly construed to disclose or suggest a metal gate formed on the insulating layer adjacent the conductive fin in a channel region of the semiconductor device, the metal gate having a thickness ranging from about 700 Å to about 2,000 Å, as required by claim 37.

For at least these reasons, the combination of Fried and Yeo does not disclose or suggest each of the features of claim 37.

In addition, even if, for the sake or argument, the combination of Fried and Yeo could be fairly construed to disclose or suggest each of the features of claim 37, Appellants submit that the motivation relied upon for combining these references does not satisfy the requirements of 35 U.S.C. § 103.

For example, the Final Office Action states that it would have been obvious to substitute a material comprising hafnium for the oxide or nitride gate dielectric layer of Fried et al. (Final Office Action – pages 3-4). This motivation is merely a conclusory statement alleging that the combination is obvious. Such a bare assertion that the combination is obvious does not satisfy the requirements of 35 U.S.C. § 103. Further, Appellants note that no portion of either reference is pointed to as providing objective motivation for the combination.

For at least these reasons, Appellants respectfully submit that the imposed rejection of claim 37 under 35 U.S.C. § 103 based on Fried and Yeo is improper. Accordingly, reversal of

the rejection of claims 37, 39-42, 46, 48, 50, and 52-54 is respectfully requested.

2. Claim 47

Claim 47 recites that the dielectric layer comprises HfSiO. Fried, as admitted in the Office Action, does not disclose a dielectric layer comprising hafnium, much less HfSiO, as required by claim 47. In addition, Yeo discloses forming a dielectric layer using HfO_2 or HfON (Yeo – col. 3, lines 31-34). Yeo does not disclose that the dielectric layer comprises HfSiO. The Final Office Action also does not disclose or suggest any reason as to why modifying either Fried or Yeo to include a dielectric material comprising HfSiO would have been obvious. Therefore, a prima facie case under 35 U.S.C. § 103 has not been established with respect to claim 47. In any event, neither Fried nor Yeo discloses or suggests this feature.

For at least these reasons, Appellants respectfully submit that the rejection of claim 47 is improper. Accordingly, reversal of the rejection of claim 47 is respectfully requested.

3. Claims 49 and 56

Claim 49 recites that the metal gate comprises a titanium nitride. The Final Office Action admits that Fried does not disclose that gate 32 of Fried comprises titanium nitride, but states that it would have been obvious to use this material since such a material is conventionally used to form gate electrodes (Final Office Action – page 3). Appellants respectfully disagree.

Claim 49 specifically recites that the metal gate for a semiconductor device that includes a silicon fin comprises a titanium nitride. Therefore, even if, for the sake of argument, titanium nitride is used to form gate electrodes for conventional MOSFET devices, Appellants assert that

titanium nitride is not conventionally used to form gates for a semiconductor device that includes a silicon fin, as required by claim 49. Appellants further assert that it would not have been obvious to use titanium nitride for the gate electrode of the combination of Fried and Yeo based on the actual disclosures of Fried and Yeo.

In other words, Appellants assert that the only motivation for using a metal gate comprising titanium nitride comes from Appellants' disclosure. Such motivation may not be properly relied upon under 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the rejection of claim 49 under 35 U.S.C. § 103 based on Fried and Yeo is improper. Accordingly, reversal of the rejection of claims 49 and 56 are respectfully requested.

4. Claims 51 and 57

Claim 51 recites that the metal gate comprises a tantalum nitride. The Final Office Action admits that Fried does not disclose that gate 32 of Fried comprises tantalum nitride, but states that it would have been obvious to use this material since such a material is conventionally used to form gate electrodes (Final Office Action – page 3). Appellants respectfully disagree.

Claim 51 specifically recites that the metal gate for a semiconductor device that includes a silicon fin comprises a tantalum nitride. Therefore, even if, for the sake of argument, tantalum nitride is used to form gate electrodes for conventional MOSFET devices, Appellants assert that tantalum nitride is not conventionally used to form gates for a semiconductor device that includes a silicon fin, as required by claim 51. Appellants further assert that it would not have been

obvious to use tantalum nitride for the gate electrode of the combination of Fried and Yeo based on the actual disclosures of Fried and Yeo.

In other words, Appellants assert that the only motivation for using a metal gate comprising tantalum nitride comes from Appellants' disclosure. Such motivation may not be properly relied upon under 35 U.S.C. § 103.

For at least these reasons, Appellants respectfully submit that the rejection of claim 51 under 35 U.S.C. § 103 based on Fried and Yeo is improper. Accordingly, reversal of the rejection of claims 51 and 57 are respectfully requested.

VIII. CONCLUSION

In view of the foregoing arguments, Appellants respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 37, 39-42, 46-54, 56 and 57.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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IX. APPENDIX

37. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin including a plurality of side surfaces and a top surface;

a source region formed on the insulating layer adjacent a first end of the conductive fin;

a drain region formed on the insulating layer adjacent a second end of the conductive fin;

a dielectric layer comprising hafnium formed on the top surface and side surfaces of the conductive fin in the channel region of the semiconductor device; and

a metal gate formed on the insulating layer adjacent the conductive fin in a channel region of the semiconductor device, the metal gate having a thickness ranging from about 700 Å to about 2,000 Å.

39. The semiconductor device of claim 37, wherein the dielectric layer has a dielectric constant greater than about 3.9.

40. The semiconductor device of claim 37, wherein the metal gate comprises at least one of titanium or tantalum.

41. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a silicon fin formed on the insulating layer, the silicon fin including a plurality of side surfaces and a top surface;

a dielectric layer comprising hafnium formed on the top surface and side surfaces of the silicon fin in the channel region of the semiconductor device;

a source region formed on the insulating layer adjacent a first end of the silicon fin;

a drain region formed on the insulating layer adjacent a second end of the silicon fin; and

a metal gate formed on the insulating layer adjacent the silicon fin in a channel region of the semiconductor device, the metal gate having a thickness ranging from about 700 Å to about 2,000 Å.

42. The semiconductor device of claim 41, wherein the silicon fin has a thickness ranging from about 300 Å to about 1,500 Å.

46. The semiconductor device of claim 41, wherein the dielectric material comprises a hafnium oxide.

47. The semiconductor device of claim 41, wherein the dielectric layer comprises HfSiO.

48. The semiconductor device of claim 41, wherein the metal gate comprises titanium.

49. The semiconductor device of claim 48, wherein the metal gate comprises a titanium nitride.

50. The semiconductor device of claim 41, wherein the metal gate comprises tantalum.

51. The semiconductor device of claim 50, wherein the metal gate comprises a tantalum nitride.

52. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin including a plurality of side surfaces and a top surface and having a thickness ranging from about 300 Å to about 1,500 Å;

a dielectric layer comprising hafnium formed on the top surface and side surfaces of the silicon fin;

a source region formed on the insulating layer adjacent a first end of the silicon fin;

a drain region formed on the insulating layer adjacent a second end of the silicon fin; and

a metal gate comprising titanium or tantalum formed on the insulating layer and over a portion of the conductive fin, the metal gate having a thickness ranging from about 700 Å to about 2000 Å.

53. The semiconductor device of claim 52, wherein the insulating layer comprises a silicon oxide having a thickness ranging from about 1,000 Å to about 3,000 Å.

54. The semiconductor device of claim 52, wherein the dielectric layer has a dielectric constant greater than 3.9.

56. The semiconductor device of claim 52, wherein the metal gate comprises a titanium nitride.

57. The semiconductor device of claim 52, wherein the metal gate comprises a tantalum nitride.

X. EVIDENCE APPENDIX

None

XI. RELATED PROCEEDINGS APPENDIX

None